Amendments to the Specification:

Please replace paragraph [0015] beginning at page 7, line 2 with the following amended paragraphs:

-- [Fig. 1] A block circuit diagram showing the internal configuration of the semiconductor integrated circuit device provided with the shift registers of a first embodiment.

[Fig. 2] A circuit diagram showing the configuration of the transistor switch.

[Fig. 3] A block circuit diagram showing another example of the internal configuration of the semiconductor integrated circuit device provided with the shift registers of the first embodiment.

[Fig. 4] A block circuit diagram showing the internal configuration of the semiconductor integrated circuit device provided with the shift registers of a second embodiment.

[Fig. 5] A block circuit diagram showing another example of the internal configuration of the semiconductor integrated circuit device provided with the shift registers of the second embodiment.

[Fig. 6] A diagram showing the configuration of the resistance that is composed of the MOS transistors and that is included in the semiconductor integrated circuit device of Fig. 5.

[Fig. 7] A block circuit diagram showing the internal configuration of another example of the semiconductor integrated circuit device provided with the shift registers of the second embodiment.

[Fig. 8] A block circuit diagram showing the internal configuration of the semiconductor integrated circuit device provided with conventional shift registers.

[Fig. 9] A timing chart partially showing the operation performed inside the semiconductor integrated circuit of Fig. [[7]] 8.

[Fig. 10] A timing chart partially showing the operation performed inside the semiconductor integrated circuit of Fig. [[7]] 8. --

Please replace paragraph [0026] beginning at page 11, line 9 with the following amended paragraphs:

-- Moreover, input terminals SI2 to SIn and input ~~drives~~ drivers Din2 to Dinn are used when data is inputted to the shift registers SR2 to SRn from the outside. Therefore, by switching ON/OFF of the switches SWA1 to SWAn-1 and the switches SWB1 to SWBn-1 according to a selection signal, it is possible to build a shift register of a desired number of bits by decoupling or coupling the shift registers SR1 to SRn. --

Please replace paragraph [0029] beginning at page 12, line 17 with the following amended paragraphs:

-- In the semiconductor integrated circuit device 1a configured as described above, the switching control portion 2 operates according to the following three states:

(1) a state in which the input terminal SI2 is not connected to the outside, and no data is inputted (a high-impedance state);

(2) a state in which high level is inputted to the input terminal SI2 as data from the outside (a high-input state); and

(3) a state in which low level is inputted to the input terminal SI2 as data from the outside (a low-input state).

(1) In a high-impedance state

In this state, low level is outputted from the switching control portion 2 as a selection signal, whereby the switch SWA turns ON, and the switch SWB turns OFF. Therefore, data outputted from the flip-flop FF64 of the shift register SR1 is inputted to the input of the flip-flop FF65 of the shift register SR2 via the switch SWA. In this way, the shift registers SR1 and SR2 are coupled together, thereby forming a 128-bit shift register.

(2) In a high-input state

In this state, high level is outputted from the switching control portion 2 as a selection signal, whereby the switch SWA turns OFF, and the switch SWB turns ON.

Furthermore, high level is inputted from the input terminal SI2 as data to the input of the flip-flop FF65 of the shift register SR2 via the input ~~drive~~ driver Din2 and the switch SWB.

(3) In a low-input state

In this state, ~~low~~ high level is outputted from the switching control portion 2 as a selection signal, whereby the switch SWA turns OFF, and the switch SWB turns ON. Furthermore, low level is inputted from the input terminal SI2 as data to the input of the flip-flop FF65 of the shift register SR2 via the input ~~drive~~ driver Din2 and the switch SWB. --

Please replace paragraph [0030] beginning at page 13, line 21 with the following amended paragraph:

-- As described in (2) or (3), when data is inputted to the input terminal SI2 from the outside, the data from the outside is inputted to the input of the flip-flop FF65 of the shift register SR2 via the switching control portion 2, the input ~~drive~~ driver Din2, and the switch SWB. In this way, the shift registers SR1 and SR2 are decoupled, thereby forming two separate 64-bit shift registers. --

Please replace paragraph [0031] beginning at page 14, line 3 with the following amended paragraphs:

-- With this configuration, as compared with the semiconductor integrated circuit device 1 of the first embodiment, the semiconductor integrated circuit device 1a of this embodiment allows the selection signal input terminal SEL that receives a selection signal to be omitted. It is to be noted that, instead of a transistor switch, a switch having a different configuration may be used as the transistor switches SWA and SWB.

(Another example of the configuration of this embodiment)

Fig. 5 shows another example of the configuration of this embodiment. With this configuration, it is possible to omit a transistor switch SWB. A semiconductor integrated circuit device 1b shown in Fig. 5 includes: resistances Ra and Rb each having one end connected to an input terminal SI2; inverters I1 to I3 each connected, on an input side thereof, to a node at which the resistances Ra and Rb are connected together; an inverter I4 that receives an output of the inverter I3; an EXOR circuit EX1 that receives outputs of the inverters I2 and I4; an inverter I5 that receives an output of the EXOR circuit EX1; an N-channel MOS transistor T1a and a P-channel MOS transistor T2a that receive, at the gates thereof, an output from the inverter I5; a ~~N~~ P-channel MOS transistor T1b and an ~~P~~ N-channel MOS transistor T2b that receive, at the gates thereof, an output of the EXOR circuit EX1; and a P-channel MOS transistor T3a and an N-channel MOS transistor T3b that receive, at the gates thereof, an output from the inverter I1. --

Please replace paragraph [0041] beginning at page 18, line 15 with the following amended paragraph:

-- With the configuration shown in Fig. 5, as compared with the semiconductor integrated circuit device 1 of the first embodiment, it is possible to omit a selection signal input terminal SEL that receives a selection signal, a transistor switch SWB, and an input ~~drive~~ driver Din2. --

Please replace paragraph [0043] beginning at page 18, line 23 as with the following amended paragraph:

-- Furthermore, as shown in Fig. 7, it may be built with n shift registers SR1 to SRn, and there may be provided with n-1 switches SWA1 to SWAn-1 and n-1 switches SWB1 to SWBn-1 between the adjacent shift registers. Moreover, the input terminals SI2 to SIn and the input ~~drive~~ drivers Din2 to Dinn are used when data is inputted to the shift registers SR2 to SRn from the outside. --

Please replace the heading at the top of page 20 with the following:

-- ~~CLAIMS~~

What is claimed is: --